

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Previously Amended) A substrate for an area array package,

said substrate having a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

said substrate having a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

said substrate having a plurality of ground via holes through the substrate, including at least one respective ground via hole through each rectangular ground plane portion,

wherein each ground plane portion has a plurality of ground via holes therethrough.

3. (Previously Amended) A substrate for an area array package,

said substrate having a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

said substrate having a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

BEST AVAILABLE COPY

said substrate having a plurality of ground via holes through the substrate, including at least one respective ground via hole through each rectangular ground plane portion,

wherein for each second contact, the respective ground plane portions are connected by a third ground plane portion on a third side of the second contact.

BEST AVAILABLE COPY

4. (Original) The substrate according to claim 3, wherein the third ground plane portion has a plurality of ground via holes therethrough.

5. (Original) The substrate according to claim 3, wherein the third ground plane portions of each second contact on at least a side of the substrate are continuously connected.

6. (Previously Amended) A substrate for an area array package,

said substrate having a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

said substrate having a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

said substrate having a plurality of ground via holes through the substrate, including at least one respective ground via hole through each rectangular ground plane portion,

wherein each pair of adjacent ones of the second contacts have a single rectangular ground plane portion therebetween.

7. (Previously Amended) A substrate for an area array package,

said substrate having a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

said substrate having a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

BEST AVAILABLE COPY

said substrate having a plurality of ground via holes through the substrate, including at least one respective ground via hole through each rectangular ground plane portion.,

wherein the substrate has an opening therethrough sized and shaped to receive the integrated circuit.

8. (Canceled)

9. (Previously Amended) An area array package comprising:
a substrate having:

a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

a plurality of ground vias through the substrate, including at least one respective ground via hole through each rectangular ground plane portion;

a cover above the substrate,

a bottom layer of the package formed of a dielectric material; and

an intermediate dielectric layer between the bottom layer and the substrate, the intermediate dielectric layer having an additional ground structure thereon.

10. (Original) The package of claim 9, further comprising a third ground structure between the bottom layer and the intermediate layer.

11. (Original) The package of claim 9, wherein the additional ground structure has a ground opening around a signal via that is coupled to the second contact, the ground opening being generally shaped like a rectangle with two mitered corners.

12. (Previously Amended) An area array package comprising:

a substrate having:

a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

a plurality of ground vias through the substrate, including at least one respective ground via hole through each rectangular ground plane portion;

a cover above the substrate, and

a bottom layer of the package formed of a dielectric material,

wherein the package has a signal via beneath each second contact, and a ground via beneath each ground via hole, each of the signal vias and ground vias being electrically connected to a respective solder attach pad on the bottom layer.

13. (Original) The package of claim 12, wherein each signal via is surrounded on three sides.

14. (Original) The package of claim 13, wherein each signal via is surrounded by at least seven ground vias.

BEST AVAILABLE COPY

15. (Previously Amended) An area array package comprising:

a substrate having:

a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

a plurality of ground vias through the substrate, including at least one respective ground via hole through each rectangular ground plane portion;

a cover above the substrate,

a bottom layer of the package formed of a dielectric material; and

a superstrate above the substrate, the superstrate generally being formed of the same material as the substrate.

16. (Original) The package of claim 15, wherein the superstrate has an opening therethrough above each second contact.

17. (Original) The package of claim 16, wherein the opening above each second contact is cylindrical and is greater in diameter than the ground vias.

18. (Original) The package of claim 16, wherein the opening above each second contact is filled with a material having a sufficiently low dielectric constant to reduce the radiation from a region of the second contact significantly.

19. (Previously Amended) An area array package comprising:

BEST AVAILABLE COPY

a substrate having:

a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the substrate,

a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, and

a plurality of ground vias through the substrate, including at least one respective ground via hole through each rectangular ground plane portion;

a cover above the substrate, and

a bottom layer of the package formed of a dielectric material,

wherein the package includes a plurality of pockets, each pocket shaped and sized to accommodate an integrated circuit.

20. (Previously Amended) A printed circuit board assembly, comprising:

a printed circuit board having a circuit board substrate with circuit traces and a plurality of devices thereon, said plurality of devices including at least one integrated circuit package assembly that includes:

a package substrate having:

a plurality of signal wirings, each having a first contact adapted to be connected to a respective terminal of an integrated circuit, and a second contact on a periphery of the package substrate,

BEST AVAILABLE COPY

a ground structure including, for each signal wiring, a pair of rectangular ground plane portions located on opposite sides of the second contact of that signal wiring, each ground plane portion having a plurality of ground via holes therethrough, and

a plurality of ground vias through the package substrate, including the plurality of ground via holes through each rectangular ground plane portion;

a lid above the package substrate, and

a bottom layer of the package formed of a dielectric material, the bottom layer having a plurality of solder attach pads, electrically connected to contacts of the circuit board substrate.

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26-31. (Canceled)

32. (Previously Added) The assembly of claim 20, wherein for each second contact, the respective ground plane portions are connected by a third ground plane portion on a third side of the second contact.

33. (Previously Added) The assembly of claim 32, wherein the third ground plane portion has a plurality of ground via holes therethrough.

BEST AVAILABLE COPY

34. (Previously Added) The assembly of claim 32, wherein the third ground plane portions of each second contact on at least a side of the substrate are continuously connected.

35. (Previously Added) The assembly of claim 20, wherein each pair of adjacent ones of the second contacts have a single rectangular ground plane portion therebetween.

36. (Previously Added) The assembly of claim 20, wherein the package substrate has an opening therethrough sized and shaped to receive the integrated circuit.

BEST AVAILABLE COPY